

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1 1. (Currently Amended) A method for managing dataflow through a
2 processing system, comprising:
3 gathering writes in a buffer before transmitting a burst of writes over an external
4 bus;
5 monitoring the buffer to determine a number of writes in the buffer and whether
6 the number of writes in the buffer exceed a predetermined threshold; ~~and~~
7 identifying an error condition when the number of writes in the buffer exceed the
8 predetermined threshold; and
9 providing control over a rate of a number of writes provided to the buffer in
10 response to the monitored number of writes in the buffer and the predetermined
11 threshold.

1 2. (Original) The method of claim 1, wherein the providing control
2 further comprises slowing writes to the buffer when the writes in the buffer exceed the
3 predetermined threshold.

1 3. (Original) The method of claim 1, wherein the gathering writes in a
2 buffer before transmitting a burst of writes over an external bus further comprises
3 transmitting a burst of writes over a bus.

1 4. (Original) The method of claim 1 further comprising initiating error
2 recovery in response to the writes in the buffer exceeding the predetermined threshold.

1 5. (Original) The method of claim 1 further comprising providing an
2 arbitration signal for controlling access to the external bus in response to the comparison
3 of the writes in the buffer to the predetermined threshold.

1 6. (Currently Amended) The method of claim 1, wherein the providing
2 control over a rate of a number of writes provided to the buffer further comprises
3 providing a vector to a register and scanning the register for the vector to determine when
4 a number of writes in the buffer is static and to slow writes to the buffer in response
5 thereto.

1 7. (Original) The method of claim 6, wherein the providing a vector to a
2 register further comprises asserting an interrupt line to the register to provide an
3 indication of an almost full state for the buffer in response to the vector.

1 8. (Original) The method of claim 1 further comprising clearing the
2 buffer when the writes in the buffer exceed the predetermined threshold.

1 9. (Original) The method of claim 1 further comprising providing a
2 timeout signal for indicating when a transaction is not cleared from the buffer within a
3 predetermined amount of time and clearing the buffer and external bus transactions in
4 response thereto.

1 10. (Currently Amended) The method of claim 1 further comprising
2 determining whether an external interface is hung based upon detecting a static buffer
3 pointer representing a lack of movement of writes in the buffer and clearing the buffer
4 and external bus transactions when an external interface is hung.

1 11. (Currently Amended) A processing system, comprising:
2 a processor for generating writes over a processor bus;
3 a buffer, coupled to the processor bus, for gathering the writes before transmitting
4 a burst of writes over an external bus; and
5 a bus monitor, coupled to the write buffer, for determining a number of writes in
6 the buffer, identifying an error condition when the number of writes in the buffer exceed
7 the predetermined threshold, and providing control over a rate of a number of writes
8 provided to the buffer in response to the monitored number of writes in the buffer and the
9 predetermined threshold comparing the number of writes in the buffer to a predetermined
10 threshold and providing a signal to the processor for causing the processor to slow writes
11 to the buffer when the number of writes in the buffer exceed the predetermined threshold.

1 12. (Original) The processing system of claim 11 further comprising an
2 external interface coupled to the buffer, the external interface linking the buffer to the
3 external bus.

1 13. (Original) The processing system of claim 11, wherein the external
2 bus comprises a PCI-X bus.

1 14. (Original) The processing system of claim 11 further comprising a
2 processor interface coupled to the buffer, the processor interface linking the buffer to a
3 processor bus.

1 15. (Original) The processing system of claim 11, wherein the processor
2 initiates error recovery in response to the writes in the buffer exceeding the
3 predetermined threshold.

1 16. (Original) The processing system of claim 11, wherein the buffer
2 monitor provides an arbitration signal for controlling access to an external bus in
3 response to the comparison of the writes in the buffer to the predetermined threshold.

1 17. (Original) The processing system of claim 11, wherein the buffer
2 monitor comprises bus arbitration and control logic for controlling the movement of data
3 onto the external bus.

1 18. (Original) The processing system of claim 17, wherein the buffer
2 bursts the writes onto the external bus.

1 19. (Currently Amended) The processing system of claim 11 further
2 comprising a register, the buffer monitor providing a vector to the register, the processor
3 scanning the register for the vector to determine when a number of writes in the buffer is
4 static and to slow writes to the buffer in response thereto.

1 20. (Original) The processing system of claim 19, wherein the buffer
2 monitor provides the vector by asserting an interrupt line to the register to provide an
3 indication of an almost full state for the buffer.

1 21. (Original) The processing system of claim 19, wherein the vector
2 represents an almost full state for the buffer.

1 22. (Original) The processing system of claim 11, wherein the buffer
2 monitor monitors the buffer, the external bus, and the processor bus for error conditions.

1 23. (Currently Amended) The processing system of claim 22, wherein the
2 error conditions comprise anticipated error conditions based upon detecting a static buffer
3 pointer representing a lack of movement of writes in the buffer.

1 24. (Original) The processing system of claim 11, wherein the buffer
2 monitor provides a buffer pointer to the processor to control the movement of writes from
3 the processor to the buffer.

1 25. (Original) The processing system of claim 11, wherein the processor
2 clears the buffer when the writes in the buffer exceed the predetermined threshold.

1 26. (Original) The processing system of claim 11, wherein the buffer
2 monitor comprises a timer for providing a timeout signal to the processor when a
3 transaction on the processor bus is not cleared within a predetermined amount of time.

1 27. (Currently Amended) A processing system, comprising:
2 a memory for gathering writes for burst transmission over an external bus; and
3 a processor, coupled to the memory, the processor being configured for
4 monitoring the memory to determine a number of writes in the buffer and whether the
5 number of writes in the memory exceed a predetermined threshold, identifying an error
6 condition when the number of writes in the buffer exceed the predetermined threshold,
7 and providing control over a rate of a number of writes provided to the memory in
8 response to the monitored number of writes in the ~~buffer~~ memory and the predetermined
9 threshold.

1 28. (Currently Amended) A program storage device readable by a computer,
2 the program storage device tangibly embodying one or more programs of instructions
3 executable by the computer to perform a method for managing dataflow through a
4 processing system, the method comprising:
5 gathering writes in a buffer before transmitting a burst of writes over an external
6 bus;
7 monitoring the buffer to determine a number of writes in the buffer and whether
8 the number of writes in the buffer exceed a predetermined threshold; ~~and~~
9 identifying an error condition when the number of writes in the buffer exceed the
10 predetermined threshold; and
11 providing control over a rate of a number of writes provided to the buffer in
12 response to the monitored number of writes in the buffer and the predetermined
13 threshold.

1 29. (Currently Amended) A processing system, comprising:
2 means for gathering writes for burst transmission over an external bus; and
3 means, coupled to the means for gathering, for monitoring the means for gather to
4 determine a number of writes in the buffer and whether the number of writes in the means
5 for gathering exceed a predetermined threshold, for identifying an error condition when
6 the number of writes in the buffer exceed the predetermined threshold, and for providing
7 control over a rate of a number of writes provided to the means for gathering in response
8 to the monitored number of writes in the buffer and the predetermined threshold.